## **WE CLAIM:**

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1. A voltage booster, comprising:

an input;

an output;

5 a boost capacitor coupled to the output; and

a pre-charge circuit operating from voltage VDD and coupled to the boost capacitor and driving the output, the pre-charge circuit having both a first NMOS transistor and a first PMOS transistor coupled between VDD and the output, wherein a gate of the first NMOS transistor is boosted above VDD to quickly charge the boost capacitor before driving the output, further comprising a third transistor selectively coupling the gate of the first PMOS transistor to the output.

- 2. The voltage booster as specified in Claim 1 wherein the third transistor couples the first PMOS transistor gate to the boost capacitor when the output is not enabled.
- 3. The voltage booster as specified in Claim 1 wherein the third transistor shunts the output to low at the moment an input voltage at the input starts going high.
- 4. The voltage booster as specified in Claim 3 wherein the third transistor gate is coupled via an inverter to the input.

- 5. The voltage booster as specified in Claim 1 wherein the third transistor allows the output to achieve a positive voltage when a non-charging side of the boost capacitor is still low.
- 6. The voltage booster as specified in Claim 1 wherein the gate of the first PMOS transistor is boosted above VDD when the input is enabled.
  - 7. The voltage booster as specified in Claim 1 wherein first NMOS transistor gate and the output are boosted above VDD at the same time.
  - 8. The voltage booster a specified in Claim 1 further comprising a second PMOS transistor coupled back-to-back with the PMOS first transistor.
- 10 9. The voltage booster as specified in Claim 1 further comprising a second NMOS transistor coupled back-to-back with the NMOS first transistor.
  - 10. The voltage booster as specified in Claim 1 wherein the first NMOS transistor has a higher drive ability than the first PMOS transistor.
- 11. The voltage booster as specified in Claim1 wherein the gate of the first NMOS transistor is coupled to the output and is boosted when the output is boosted.
  - 12. The voltage booster as specified in Claim 1 wherein the third transistor is a PMOS transistor.
- 13. The voltage booster as specified in Claim 1 further comprising a fourth transistor coupling the input to the gate of the first PMOS transistor.
  - 14. The voltage booster as specified in Claim 13 wherein the gate of the fourth transistor is coupled to VDD.

- 15. The voltage booster as specified in Claim 13 wherein the fourth transistor discharges the gate of the first PMOS transistor when the output is disabled.
- The voltage booster as specified in Claim 15 wherein the fourth
  transistor also isolates the gate of the first PMOS transistor from the output when the output is enabled.
  - 17. The voltage booster as specified in Claim 1 further comprising a memory device wherein the output is coupled to and drives a word line of the memory device.
- 10 18. The voltage booster as specified in Claim 17 wherein the output is boosted above VDD during a memory access.
  - 19. The voltage booster as specified in Claim 18 wherein the first PMOS device drives the output initially during the memory access.
- The voltage booster as specified in Claim 19 wherein the first
  PMOS transistor keeps the voltage at the output at VDD during standby.
  - 21. The voltage booster as specified in Claim 17 further comprising a first capacitor coupled to and boosting the gate of the first NMOS transistor.